Di Wang

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EDUCATION

- **University of California, Berkeley** *August 2023 - Present*
  PhD in Electrical Engineering & Computer Sciences (Integrated Circuit Design) Berkeley, CA
  - GPA: 3.970/4.00
  - Research Focus: Time-Domain Clocking Techniques for Low-Power Die-to-Die Parallel Link Applications
  - Advisor: Prof. Borivoje Nikolić [🌐]
  - Relevant Coursework:
    - **Circuit Design:** Intro to Digital Design (A+), Advanced Analog IC (A+), Data Converters (A+)
    - **Control Theory:** Nonlinear Control (A+), Linear Control Systems (A), Stochastic Processes (A)
- **Nanyang Technological University, Singapore** *August 2019 - June 2023*
  Bachelor of Engineering, Electrical and Electronic Engineering Singapore
  - GPA: 4.85/5.00 | Honours (Highest Distinction)
  - Specialization: Electronic Engineering (Integrated Circuit Design)
  - Dean's List: 2019-2020, 2020-2021
  - IEEE Solid-State Circuits Society Singapore Chapter Undergraduate Student Prize

SKILLS

- **Programming:** C/C++, Python, MATLAB, Verilog HDL
- **Circuit Design:** Analog/Mixed-Signal circuit design and layout, System modeling and simulation
- **EDA Tools:** Cadence, Synopsys, Mentor Graphics Digital + Custom Signoff tools
- **Process Technologies Used + Taped-out:** TSMC 65nm, 7nm, 4nm, 3nm, Intel 16FFL, Skywater 130nm

PROJECTS

- **Supply-Tolerant Clocking Design for UCIe Protocol Implementation** *September 2025 - Present*
  TSMC N7 PDK
  - Developing supply-tolerant PLL and clock distribution techniques to enhance voltage noise robustness
  - Designing deskew system architecture to achieve tight jitter tracking specifications
  - Leading full chiplet tape-out (2.5×2.5 mm^2) in TSMC N7 for 2026Q3 university shuttle
- **UCIe Chiplet Protocol Implementation for High-Speed D2D Interconnect** *January 2024 - January 2026*
  Intel 16FFL PDK
  - Designed 8GHz Sub-Sampling Digital PLL achieving 518fs RMS jitter
  - Developed prototype deskew lane with DLL, PI, and DCC achieving 0.916ps RMS jitter
  - Chips taped-out in Intel 16FFL 2024Q3 and 2025Q2 university shuttles
  - Measured 5.4pJ/b energy efficiency at 256Gb/s data rate in silicon, and 14.4Gb/s/lane using the designed PLL and deskew system
- **AcceLeNetor: FPGA-Accelerated Neural Network Implementation** *August 2022 - June 2023*
  Undergraduate Final Year Project [🐙]
  - Implemented CNN accelerator in Verilog HDL for handwritten digit recognition on FPGA
  - Ported CNN to ChipWhisperer for power analysis and hardware reverse engineering of network structures
- **NTU High-Performance Computing Team** *March 2021 – November 2022*
  System Administrator and Hardware Engineer
  - Managed HPC cluster with 3 nodes and 11 A100 GPUs
  - Achieved 2nd place in SC22 Student Cluster Competition in Dallas, TX, US [🌐]

Experience

- **Apple Inc. [🌐]** *May 2025 - August 2025*
  SerDes Micro-Architecture Intern Beaverton, OR, US
  - Designed and optimized high-speed SerDes PHY circuits including PLL, clock distribution, and lane components
  - Performed circuit-level simulations and Monte Carlo analysis to achieve jitter and power targets
  - Collaborated with architecture and physical design teams on full chip integration
- **A*STAR: Institute of Microelectronics (IME) [🌐]** *June 2023 - July 2023*
  Analog/Mixed-Signal Design Engineering Intern Singapore
  - Designed cryogenic temperature sensors for quantum computing applications using TSMC 65nm PDK
- **MediaTek Singapore Pte Ltd [🌐]** *December 2021 - May 2022*
  GPU/APU Design Verification & Implementation Engineering Intern Singapore
  - Performed logic synthesis and resolved timing violations in GPU/APU designs
  - Collaborated with RTL and physical design teams to optimize floorplan implementation
- **Fourth Paradigm Southeast Asia Pte Ltd [🌐]** *May 2021 - August 2021*
  FPGA Research Development Intern Singapore
  - Contributed to Persistent Memory (PMEM) research for improving Kafka stability and performance

Publications and Papers

C=Conference, J=Journal, P=Patent, S=In Submission

[S.1] Rahul Kumar*, Rohan Kumar*, **Di Wang***, Nikhil Jain, Oliver Yu, Bob Zhou, Kevin Anderson, Vikram Jain, Borivoje Nikolić (2026). **An Open-Source, Programmatically-Generated 5.4pJ/b 256Gb/s UCIe-Compatible PHY in Intel 16**. In submission.

[S.2] **Di Wang**, Borivoje Nikolić (2026). **Loop Latency Analysis and Hybrid KP Sizing for Wide-Bandwidth Bang-Bang PLLs**. Under review for journal publication.

[C.1] Kevin Anderson*, **Di Wang***, Rahul Kumar, Rohan Kumar, Ella Schwarz, Mahsa Sadeghi, Miles Rusch, Lux Zhang, Yufeng Chi, Dima Nikiforov, Daniel Lovell, Jerry Zhao, Vikram Jain, Yakun Sophia Shao, Krste Asanovi, Borivoje Nikoli (2026). **KODIAK: RVV Vector Processor Chiplet Featuring Outer-Product Matrix Engine, Chip-to-Chip Link, and UCIe Interface in Intel16**. In *European Solid-State Electronics Research Conference (ESSERC'26)*.

[C.2] Vikram Jain, Hasan Genc, Coleman Hooper, Minh Nguyen, Rahul Kumar, Rohan Kumar, **Di Wang**, Kevin Anderson, Yufeng Chi, Kris Dong, Dima Nikiforov, Bob Zhou, Borivoje Nikolić, Sophia Shao (2026). **Sirius: A Dual-Chiplet System for Multimodal Embodied AI with Heterogeneous RVV Cores, Dense and Sparse Accelerators**. In *Symposium on VLSI Technology & Circuits (VLSI'26)*.