Latency Compensation Techniques for Wide-Bandwidth Phase-Locked Loop Systems

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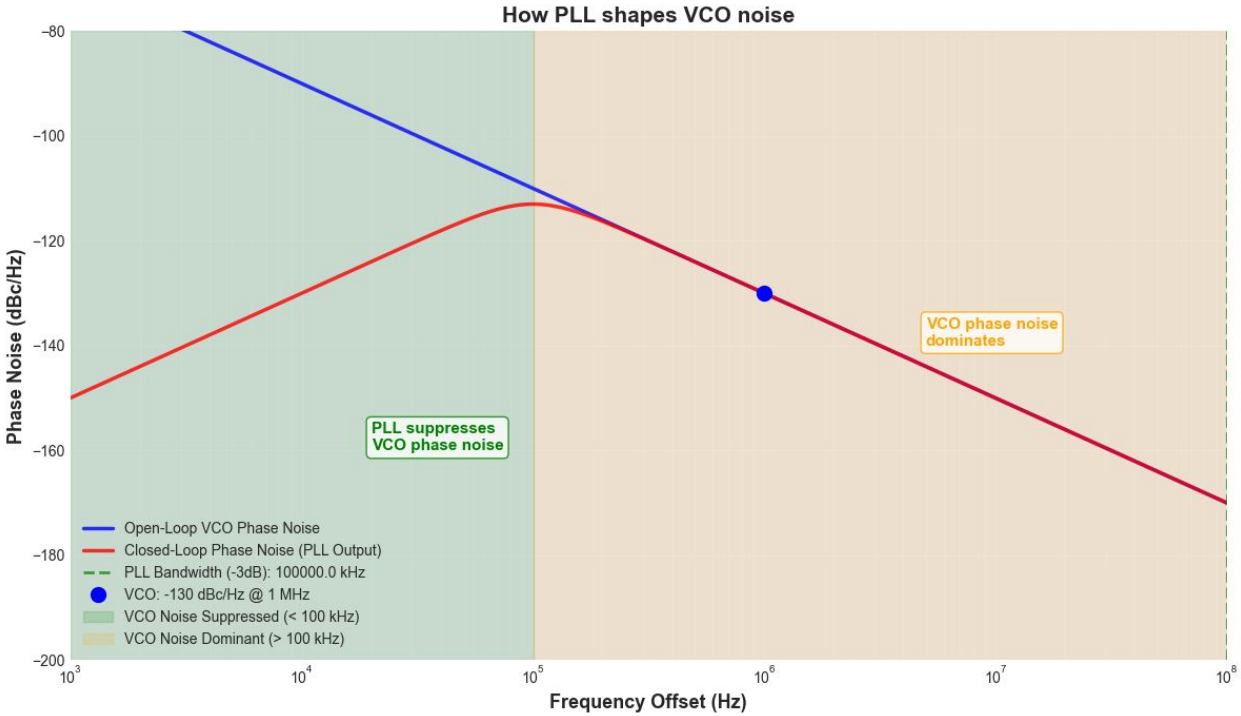
Overview

- **Motivation**
  - Why wide-bandwidth PLL
  - Why low latency matters
- **SSDPLL for UCIe application**
- **Problems with SSDPLL and other digital PLLs**
- **BBPLL analysis**
  - Architecture
  - Loop analysis and noise analysis
- **Proposed hybrid Kp PLL**
  - Architecture
  - Loop analysis
  - Charge pump design
  - Closed loop verification

Motivation: Wide Bandwidth

1. Suppression of open-loop oscillator noise
2. Rejects frequency pulling and offer faster locking
3. Improves jitter tolerance, if used as CDR



Motivation: Low Latency

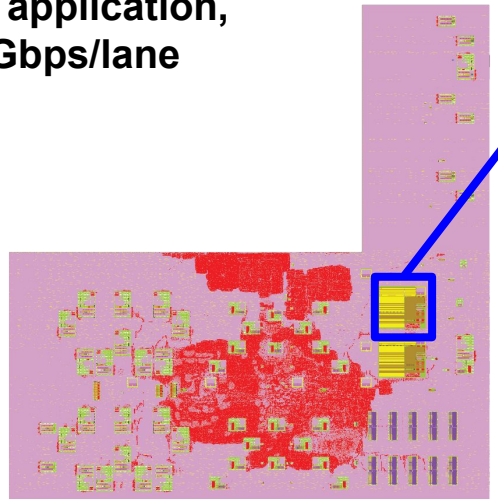
- **A design metric for a closed loop PLL is the phase margin (PM)**
  - Usually, people choose PM around 60 to 70 degrees for stability and fast settling
- **Latency, if modeled in a linear loop, shows as a phase shift term:**

$$\Delta\Phi_M = -2\pi f_{\mathrm{BW,unity}} \Delta T$$

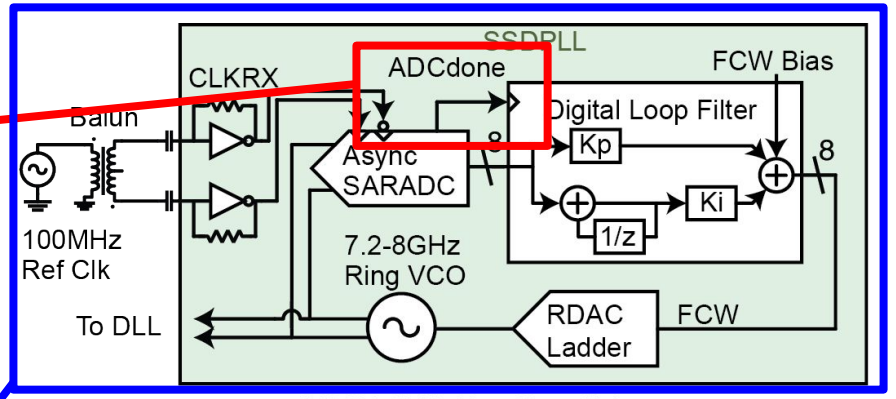
- **Large delay will reduce phase margin**
  - Small phase margin causes large ringing
  - Negative phase margin causes the system to go unstable
- **For wide bandwidth PLLs, f_BW is large, so phase margin is more vulnerable to latencies**

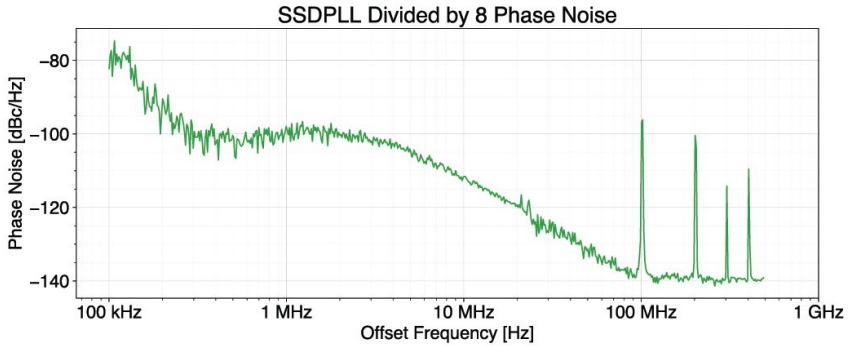
SSDPLL for UCIe application

- **Sub-Sampling Digital PLL**
- **Use asynchronous SARADC's done signal to trigger DLF update asap**
- **PLL taped-out and used to clock UCIe die-to-die application, achieving 14.5Gbps/lane performance**



UCIe die shot





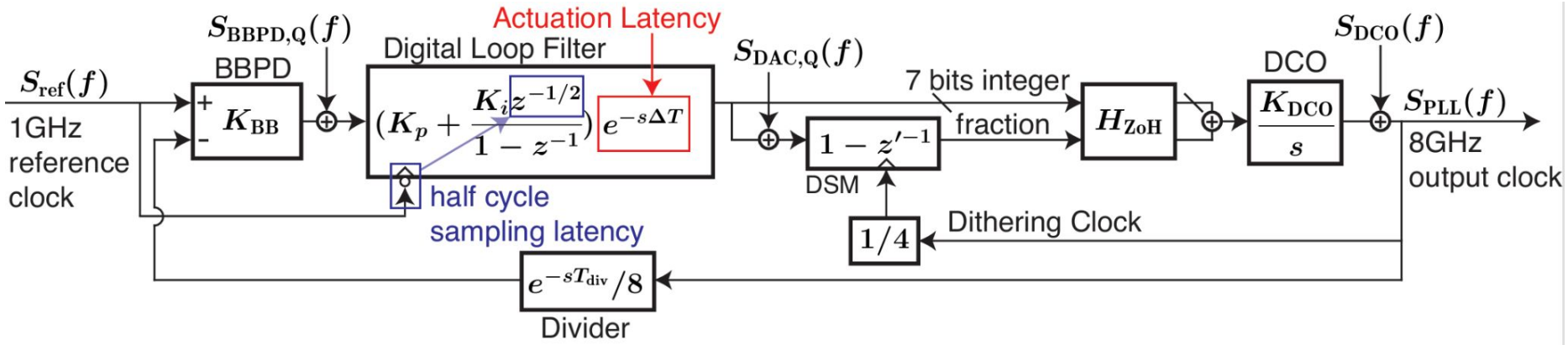
SSDPLL illustration

Problems with SSDPLL and other digital PLLs

- **SSDPLL requires a wide-bandwidth 4-8bits ADC which is power hungry and not scalable**
- **Main latency contributor is not from SARADC, but from DLF's actuation latency**
  - Propagation delay, retiming activity
- **Comparison between some potential PLL architecture candidates**
  - PFD + CP PLL
    - 👍 Great for low latency
    - 👎 can't achieve high gain
  - Sub-sampling PLL (analog)
    - 👍Can achieve large gain and low latency
    - 👎 have harmonic locking problem + limited linear range
  - Bang-Bang PLL
    - 👍 Can achieve large gain
    - 👍👍👍 simple, effective, scalable!
    - 👎 suffer from both latency and BB quantization noise
    - ❓ Can we do one optimization to resolve the latency + BB quantization noise problem?

Bang-Bang PLL Architecture

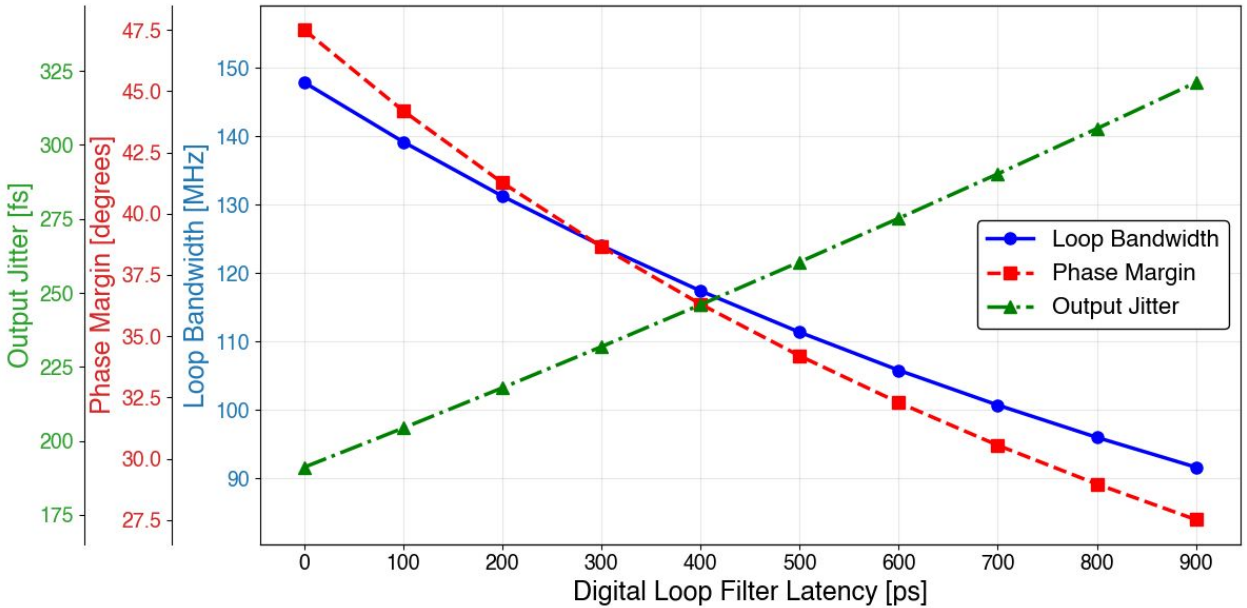
- Typical BBPLL block diagram
- Consider using a ring oscillator with -15dBc/Hz @ 10kHz, -130dBc/Hz @ 1MHz noise
- Use 1GHz ref clock to achieve 150MHz unity gain bandwidth for 8GHz output clock
- Actuation latency: 520ps
- Output jitter target: < 200fs (1kHz - 4GHz)
- We vary actuation latency, and check how that affects the loop performance



Bang-Bang PLL Latency Analysis: Loop Dynamics

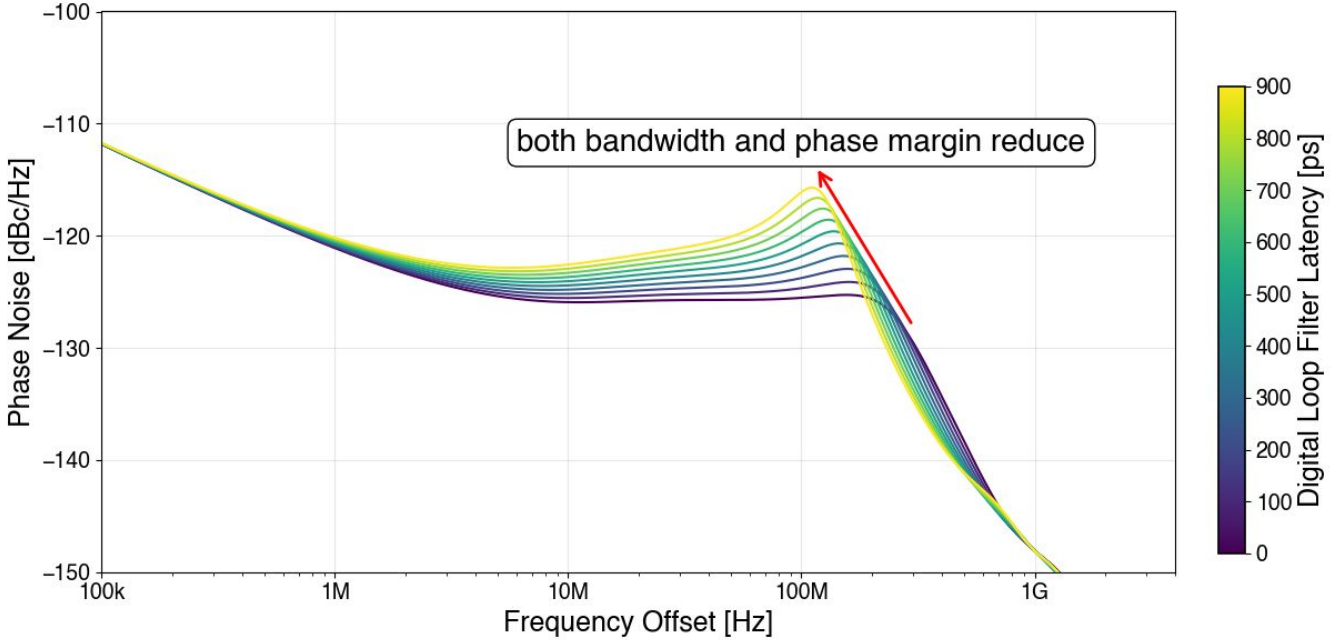
- For a linear PLL, latency is a phase shift, doesn't affect loop bandwidth
- For a BBPLL, latency affects loop phase margin, affecting jitter, affecting BBPD gain, affecting loop bandwidth
- Use a numeric solver to find how actuation latency affects the BBPLL

$$\begin{cases} K_{\mathrm{BB}}(\sigma_{j,\mathrm{PLL}}) &= \dfrac{2}{\sqrt{2\pi(\sigma_{j,\mathrm{PLL}}^2+\sigma_{j,\mathrm{ref}}^2)}} \\ LG_{\mathrm{delay}}(s) &= K_{\mathrm{BB}}(\sigma_{j,\mathrm{PLL}})\left(K_p+\dfrac{K_i e^{-s(T_{\mathrm{ref}}/2)}}{1-e^{-sT_{\mathrm{ref}}}}\right) H_{\mathrm{ZoH}}(s)\cdot\dfrac{K_{\mathrm{DCO}}}{s}\dfrac{e^{-s(T_{\mathrm{div}}+\Delta T)}}{8} \\ \sigma_{j,\mathrm{PLL}} &= \dfrac{1}{\omega}\sqrt{\sum_{i\in\{\mathrm{DCO,\ ref,\ BBPD\_q,\ DCO\_q}\}}\int_{1\mathrm{kHz}}^{4\mathrm{GHz}}|NTF_i(s)|^2 S_i(f)\,df} \end{cases}$$



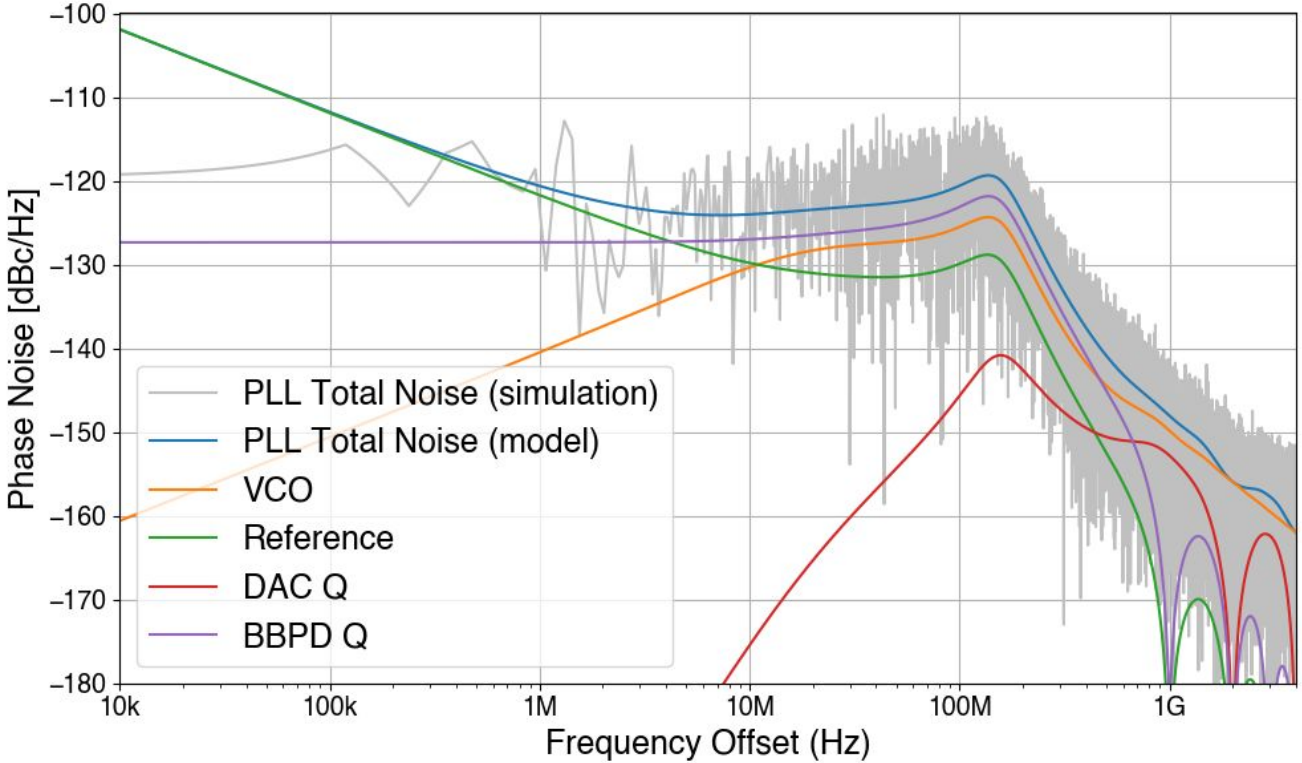
Bang-Bang PLL Latency Analysis: Phase Noise Plot

- **As a result from bandwidth and phase margin reduction, we see more peaking in BBPLL phase noise plot**



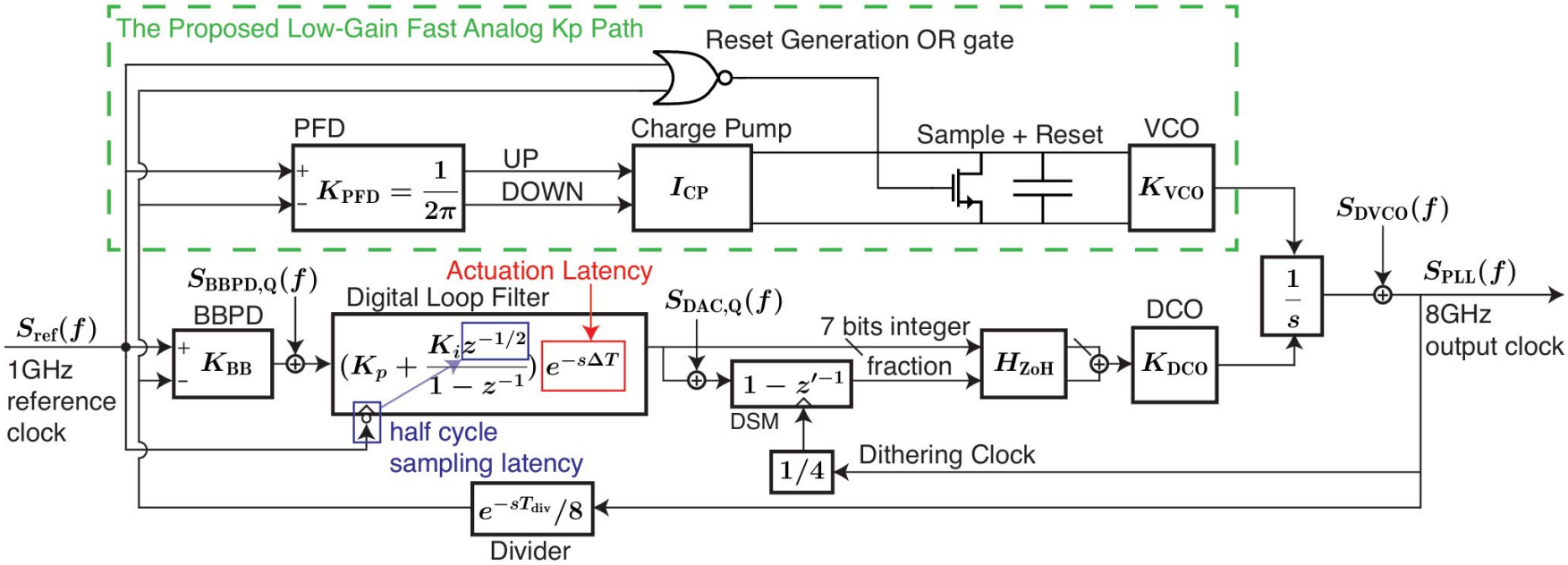
Bang-Bang PLL Phase Noise Performance

- **At 520ps latency, BBPLL integrated jitter = 263fs**
- **BBPD Quantization noise dominates around bandwidth**



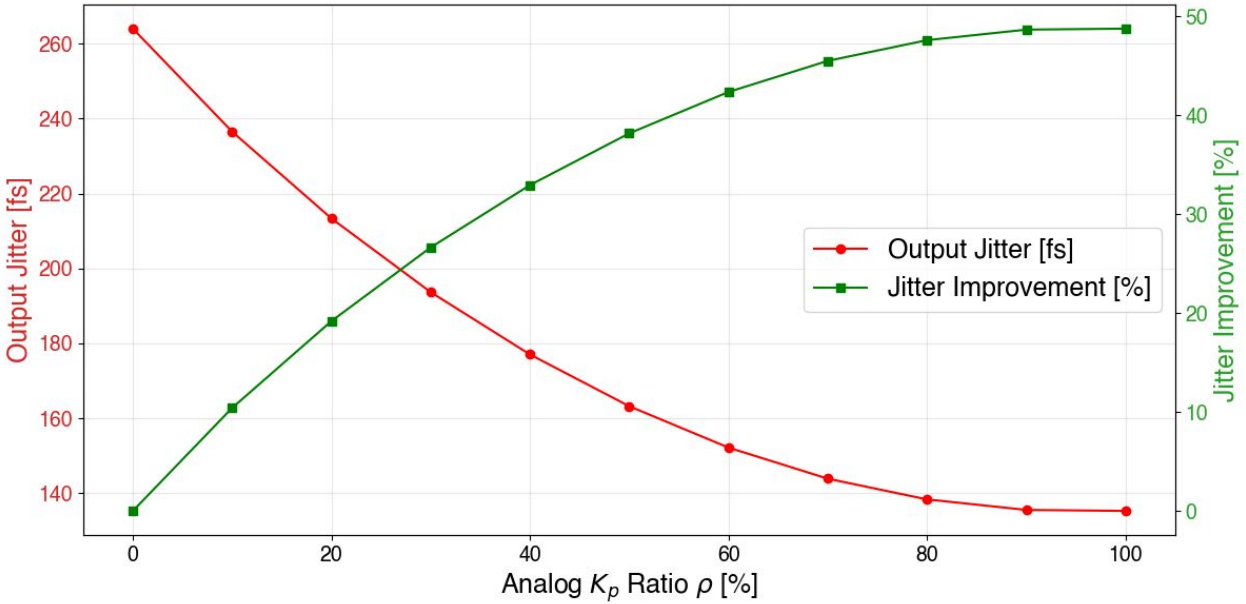
Proposed Hybrid Kp PLL

- **We introduce a fast, low gain, linear analog Kp path to resolve BBPD quantization noise and latency problem**



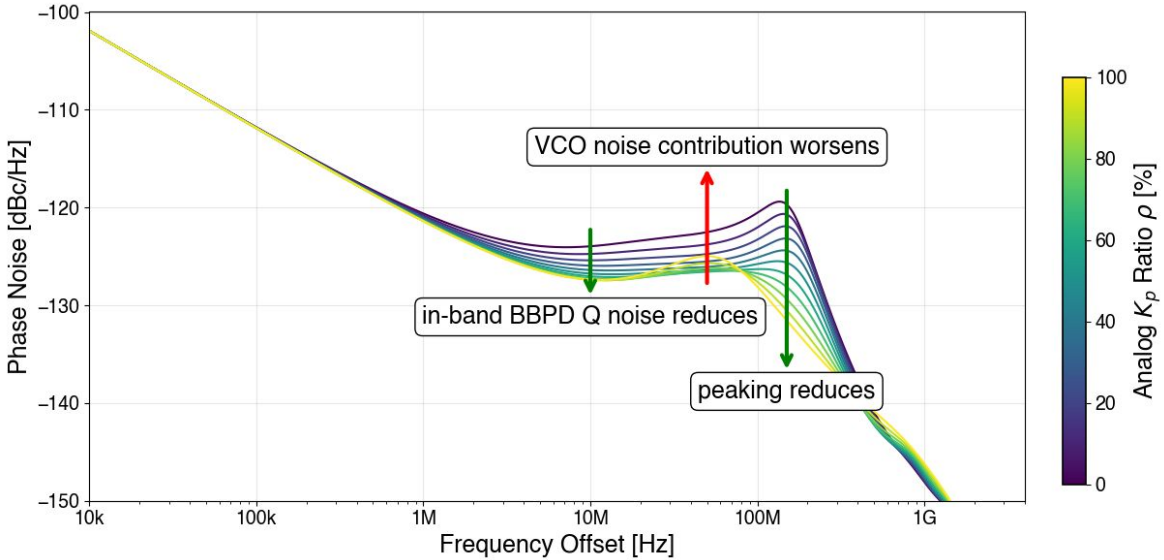
How should I set the analog Kp gain? (jitter improvement)

- We define the ratio between analog Kp path gain versus the overall gain
- We see general improvement in the output jitter, but the return is diminishing
- Rule of thumb: 30% of analog Kp ratio leads to 50% of the overall jitter improvement
- The greater the latency is, the more effective analog Kp gain is



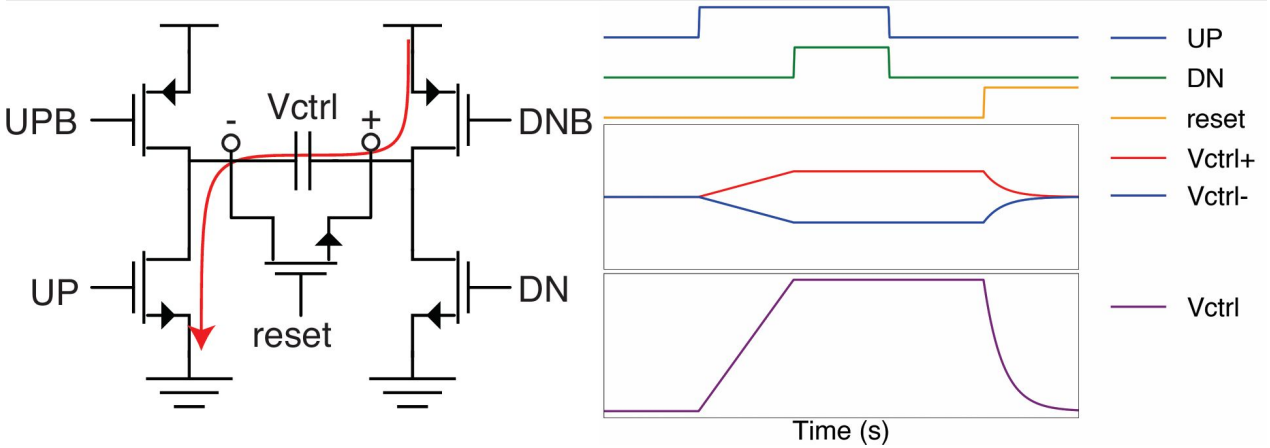
How should I set the analog Kp gain? (phase noise)

- **Why do we have a diminishing return in jitter reduction?**
  - When increasing analog gain ratio, peaking reduction happens first, and in-band BBPD Q noise reduction happens later
  - BBPD Q noise is in band, which is less significant



Analog Kp gain provider: Switched Capacitor Charge Pump

- Don't want complex analog circuit, otherwise defeat out scalable purpose
- Use simple current steering differential capacitor to achieve fast response
- Use PFD in front to sense the phase difference



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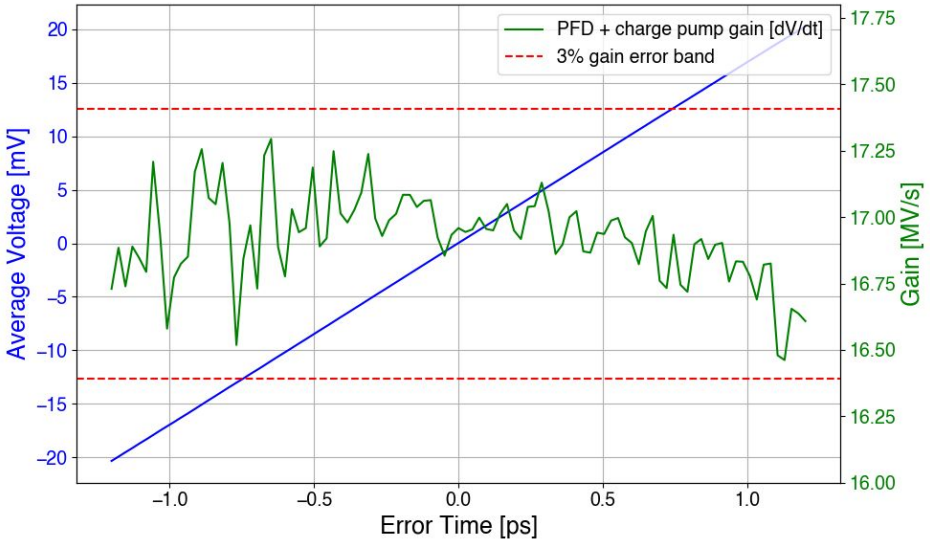
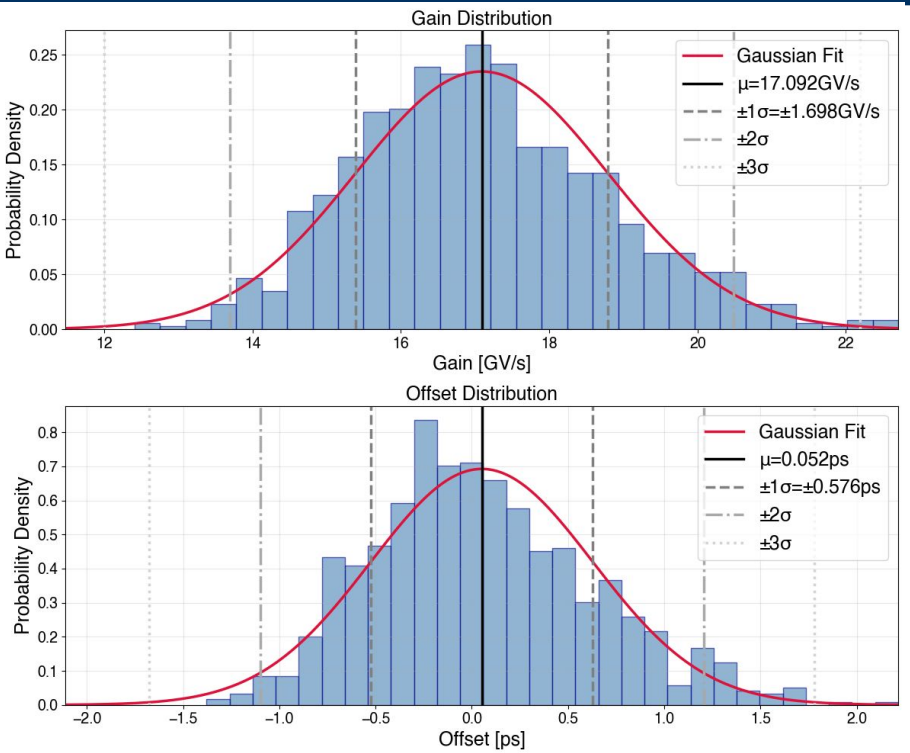


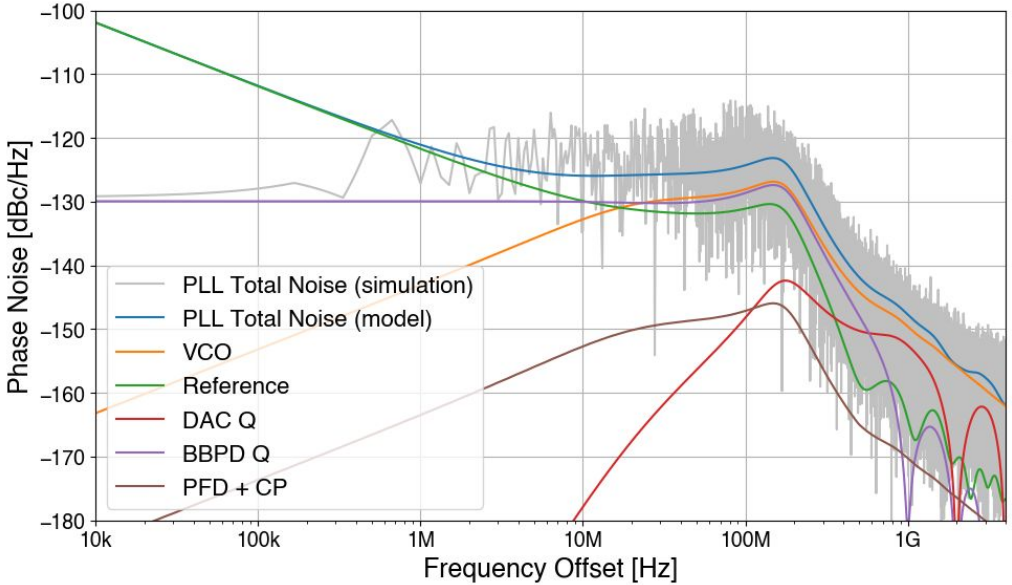
Gain Plot

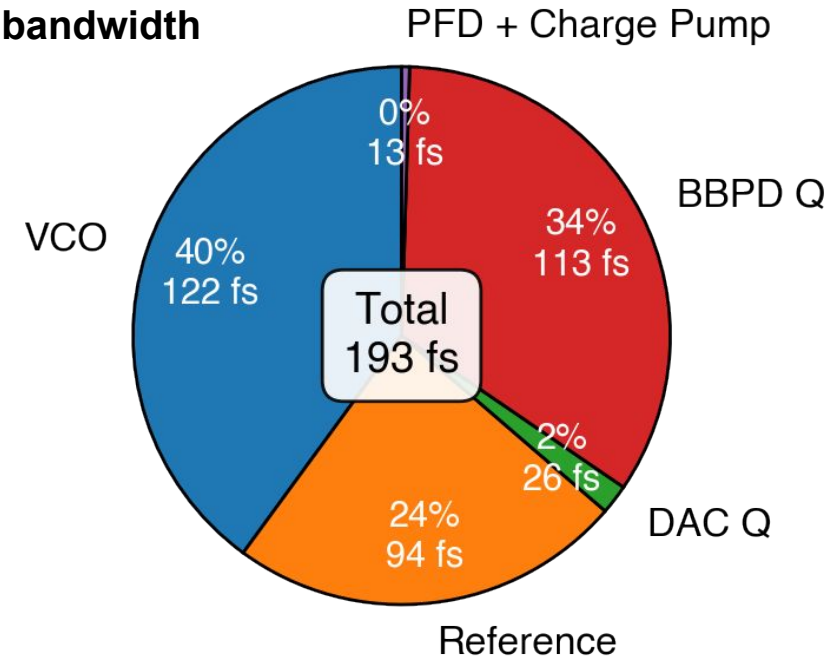


Monte Carlo Plot

Closed Loop Simulation

- **PFD + Charge Pump adds minimal phase noise, minimal complexity, but reduces jitter from 263fs down to 193fs**
- **BBPD Q noise no longer dominates around bandwidth**





Conclusion

- **Wide-bandwidth PLLs are favored in modern communication systems**
  - Whereas latency is a more severe problem for WBPLLs than LBPLLs
- **We discussed some design considerations**
  - SSDPLL
    - Useful if ADC sampling latency matters, but expensive
  - BBPLL
    - High gain, but high latency
    - Analyzed how latency affects the loop performance
  - Hybrid Kp controlled PLL
    - Introduce a fast low-gain path for latency compensation
    - Simply analog gain circuit, scalable, addes low phase noise to the output
    - Reduces both phase noise peaking and BBPD phase noise